REMARKS

Applicant appreciates the Examiner's thorough examination of the subject application and requests reconsideration of the subject application based on the foregoing amendments and the following remarks.

Claims 1-21 are pending in the subject application.

Claims 1-21 stand rejected under 35 U.S.C. §103.

Claims 22-26 were added to more distinctly claims aspects/ embodiments of the present invention. The amendments to the claims are supported by the originally filed disclosure.

35 U.S.C. §103 REJECTIONS

Claims 1-21 stand rejected under 35 U.S.C. §103 as being unpatentable over the cited prior art for the reasons provided on pages 2-6 of the above-referenced Office Action. The following addresses the specific rejections provided in the above-referenced Office Action.

CLAIMS 1-13, 16-17, 20 & 21

Claims 1-13, 16-17 20 and 21 stand rejected under 35 U.S.C. §103 as being unpatentable over over Suzuki et al. [USP 6,445,367; "Suzuki"] in view of Lill [USP 5,394,442] and Yoshida [USP 5,889,817; "reference"] for the reasons provided on pages 2-5 of the above-referenced Office Action. Applicant respectfully traverses as discussed below.

As grounds for the rejection the above-referenced Office Action asserts that Suzuki teaches a control circuit (103) through which an image signal enters from the outside and which generates control signals, Tscan and Tmry, that are applied to a latch circuit (105). It is further asserted that the latch circuit (105) is used as a memory circuit for storing one line of the image data for a certain period of time only. It also is asserted that Suzuki teaches a shift register that is used for converting the image data, which enters serially in a time series to parallel signals every line of the image.

The Office Action, however, admits that Suzuki does not teach the storage means of the present invention that stores, as the digital data, a digital data which is a single signal of serial data including a time series of data pulses representative of all rise and fall timings of the plurality of kinds of pulse signals and data pulses representative of all time intervals between the rise and falling timings. The Office Action does further assert that Lill provides the necessary teachings and that it would have been obvious to one skilled in the art to modify Suzuki's system of data processing to adapt Lill's storages. Applicant respectfully disagrees with this characterization of the teachings of Lill and further that one skilled in the art would have been motivated to modify the control circuit 103 in Suzuki so as to incorporate the storages of Lill.

The Office Action, however, also admits that Suzuki also does not teach the serial-parallel converting means of the present invention that reads the storage means and producing as parallel data. It is asserted that Yoshida provides the missing teachings and that it would have been obvious to one skilled in the art to modify Suzuki's image forming apparatus to include

Yoshida's use of serial/ parallel conversion circuit 1011. Applicant respectfully disagrees with this characterization of the teachings of Lill and further that one skilled in the art would have been motivated to modify the control circuit 103 in Suzuki so as to incorporate the serial/ parallel conversion circuit of Yoshida.

Applicant claims, claim 1, a signal production circuit for producing a plurality of kinds of pulse signals as well as claims, claim 9, a display device including such a signal production circuit, which signal production circuit includes, *inter alia*: (1) *storage means* for storing, as digital data, a single signal of serial data including a time series of data pulses representative of all rise and fall timings of the plurality of kinds of pulse signals and data pulses representative of all time intervals between the rise and fall timings; and (2) *serial-to-parallel converter means* for reading the signal of serial data from the storage means and producing, as parallel data, the plurality of kinds of pulse signals from the data representative of all the predetermined rise and fall timings of the plurality of kinds of pulse signals. It necessarily follows from the foregoing that the storage means is operably coupled to the serial-to-parallel converter means such that the signal of serial data stored in the storage means can be read by the serial-to-parallel converter means such that the signal of serial data is converted within the converter so as to produce the plurality of parallel signals therefrom.

As to Lill, this reference teaches a receiving section coupled to a fiber optic transmission medium. Also, the invention in Lill relates to digital data transmission systems in which clock

information, data and other information is transmitted within a single band and more particularly such systems that are used with optical communication mediums.

The Office Action asserts or alleges that Lill teaches four pulses (P1 to P4) stored in RTS control signal storage register and in data storage register, and that Lill also teaches edge triggered storage registers (60, 64) storing outputs from digital timers (58, 62).

Lill teaches that a composite signal has four pulses (P1 to P4), which constitute a frame of the digital signal to be transmitted (see col. 3, lines 60 to 67 thereof). Lill also teaches that the storage register 20 produces the DATA FF1 signal that is sampled once per frame at the center of the frame. The data FF1 signal is the pulse identified by the legend P4 in Fig. 3a (see col. 4, lines 40 to 55 thereof). The signals S2 and S4 are high-level bits that occur within the frame, and are used for transmitting any type of information other than information for controlling the clock of the receiver (see col. 4, lines 1 to 5 thereof). Moreover, it is clearly described in Lill (see col. 4, lines 31 to 36, thereof) that the storage register 20 latches the data signal which is to be sent a bit at a time.

From the above disclosures/ teachings in Lill, Applicant submits that the storage register 20 only latches inputted basic data signal and generates the pulse P4, which is one of the four pulses. As such, it is respectfully submitted that the storage register 20 *does not* store "data pulses representative of all rise and fall timing of the plurality of kinds of pulse signals" of the presently claimed invention.

As to the edge triggered storage registers (60, 64), Lill only discloses that the edge triggered storage registers (60, 64) sample "additional bits DC1 to DCAn" after the clocking operation of the digital timers 58 and 62. Moreover, it also is disclosed in Lill that the digital timers 58 initiate storage of the bit level present at the bit positions of the MES signal (see col. 6, lines 17 to 20 thereof).

Thus, the digital timers 58 and 62 are mere timers that start clocking operations in accordance with clocking start instructions, respectively, and, after a predetermined time, output respective binary signals for initiating the storage of the bit level. Therefore, the outputs of the digital timers 58 and 62 are not "data pulses representative of all time intervals between the rise and fall timing" of the presently claimed invention.

In sum, it is clear from the foregoing remarks that Lill does not disclose nor suggest the storage means for storing, as the digital data, a single signal of serial data including a time series of data pulses representative of all rise and fall timing of the plurality of kinds of pulse signals and data pulses representative of all time intervals between the rise and fall timing of the presently claimed invention. As such, it can hardly be said that combining the teachings of Lill with the disclosures of Suzuki, would have yielded the signal production circuit of claim 1 or the display device of claim 9.

It also is asserted in the Office Action, that Yoshida teaches a 16 bit shift register (1012) that is provided between a Manchester decoding circuit (1010) and a serial/ parallel conversion circuit (1011) and is further asserted that it would have been obvious to one skilled in the art at

the time the invention was made to modify the image forming apparatus disclosed in Suzuki to include Yoshida's use of serial/ parallel conversion circuit 1010).

The serial-to-parallel converter means of the present invention reads serial data contained in the storage means, and generates parallel pulse signals of different kinds based on the rise and fall timings of the serial data. That is, the function of the serial-to-parallel converter means of the present invention is not merely to rearrange data but to generate pulse signals based on the rise and fall timings of serial data. Thus, in this respect, the serial-to-parallel converter means of the present invention is clearly different, both structurally and functionally, from the serial/ parallel conversion circuit 1011 of Yoshida.

This assertion also appears to be predicated on the fact that the Manchester encoding technique would equivalently provide the desired single signal incorporating the time series of data pulses. As indicated above, the Manchester encoding technique does not change the form of the parallel data stream so as to be a signal of serial data as is set forth in the claims as well as the subject application. Rather it is a data encoding technique whereby a parallel data stream is reformatted so as to produce another parallel data stream having a different bit rate from the first data stream (*i.e.*, double the bit rate of the first data stream). As such, it necessarily follows that the use of the Manchester encoding technique in Yoshida also would **not** equivalently provide the desired single signal incorporating the time series of data pulses.

Applicant respectfully submits that, as was commented on by Applicant in the previously submitted Response, the serial-to-parallel converter means of the present invention can not be conceived on the basis of Manchester phase encoding nor the teachings of Yoshida.

Applicant would note that limiting the foregoing remarks to the disclosures and teachings of Lill and Yoshida *should not be interpreted as* or be understood to be a *waiver* of any argument *as to the appropriateness of the suggested combination* of Suzuki and the teachings of Lill and/ or of Suzuki and the teachings of Lill and Yoshida *ab initio*. Applicant believes that Examiner has not provided a sufficient basis as to why one skilled in the art, *absent the disclosures and teachings of the subject application*, would have even considered the teachings of Lill and/ or Yoshida much less adapt and modify the teachings of Lill and Yoshida so that these teachings would lead one skilled in the art to modify the display apparatus and related circuits disclosed in Suzuki so as to provide the signal production circuit of the present invention or a display apparatus embodying such a signal production circuit.

In this regard and with reference to the foregoing discussion regarding Lill and Yoshida, Applicant would note that Lill does not teach the storage means of the present invention nor the serial-to-parallel converter means of the present invention, and the same holds true for Yoshida. Therefore, it necessarily follows that not only can neither Lill nor Yoshida make up for what Suzuki fails to disclose, there can be no reasonable ground asserted or proffered for combining Suzuki, Lill, and Yoshida as well.

As provided in MPEP 2143.01, obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. *In re Fine*, 837 F. 2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988); *In re Jones*, 958 F. 2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). As provided above, the references cited, alone or in combination, include no such teaching, suggestion or motivation.

Furthermore, and as provided in MPEP 2143.02, a prior art reference can be combined or modified to reject claims as obvious as long as there is a reasonable expectation of success. *In re Merck & Co., Inc.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 19866). Additionally, it also has been held that if the proposed modification or combination would change the principle of operation of the prior art invention being modified, then the teachings of the references are not sufficient to render the claims *prima facie* obvious. Further, and as provided in MPEP-2143, the teaching or suggestion to make the claimed combination and the reasonable suggestion of success must both be found in the prior art, not in applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). As can be seen from the forgoing discussion regarding the disclosures of the cited references, there is no reasonable expectation of success provided in the references. Also, it is clear from the foregoing discussion that the modification suggested by the Examiner would change the principle of operation of the circuitry disclosed in Suzuki.

As the Federal circuit has stated, "[t]he mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification." *In re Fritch*, 972 F.2d 1260,1266, 23 USPQ2d 1780, 1783-84 (Fed. Cir. 1992). Obviousness may not be established using hindsight or in view of the teachings or suggestions of the inventor. *Para-Ordance Mfg. v. SGS Importers Int'l, Inc.*, 73 F.2d 1085, 1087, 37 USPQ2d 1237, 1239 (Fed. Cir. 1995).

As the CAFC has stated a number of times, the examiner can satisfy the burden of showing obviousness of the combination only by showing some objective teaching in the prior art or that knowledge generally available to one of ordinary skill in the art would lead that individual to combine the relevant teachings of the references. In other words, the Examiner has an obligation to specifically show an applicant the reason by which a person of ordinary skill in the art would have selected and combined the references that are being asserted against the claims of an applicant without any knowledge of an applicant's disclosure. As the CAFC also has indicated the best defense against the subtle but powerful attraction of a hindsight-based obviousness analysis is rigorous application of the requirement for a showing of the teaching or motivation to combine prior art references. See e.g., *In re Dembiczak*, 50USPQ2d 1614 (Fed. Cir. 1999); *In re SANG-SU LEE*, 271 F.3d 1338, 1342-1344; 277 USPQ 2d 1430 (Fed. Cir. 2002).

It is respectfully submitted that the foregoing remarks regarding claims 1 and 9 also apply to distinguish each of claim 7, 8, and 10-13 from the combination or references.

It is respectfully submitted that claims 1-13, 16-17, 20 and 21 are patentable over the cited reference(s) for the foregoing reasons.

CLAIMS 14-15, 18 & 19

Claims 14-15, 18 and 19 stand rejected under 35 U.S.C. §103 as being unpatentable over over Suzuki et al. [USP 6,445,367; "Suzuki"] in view of Lill [USP 5,394,442] and Yoshida [USP 5,889,817; "reference"] and further in view of Frala et al. [USP 5,001,694; "Farla"] for the reasons provided on pages 5-6 of the above-referenced Office Action. Applicant respectfully traverses as discussed below.

Each of claims 14-15 and 18 depend directly or ultimately from claim 1. As indicated in the discussion above, the signal production circuit of claim 1 is not disclosed, described, taught or suggested in the combination of Suzuki, Lill and Yoshida. Applicant also submits that this combination of references also does not provide any teaching, suggestion nor offer any motivation for modifying the signal production circuitry disclosed in Suzuki so as to yield the signal production circuitry of claim 1. As such, at least because of their dependency from a base claim that is believed allowable, each of claims 14-15, and 18 also are believed to be allowable.

Claim 18 also depends from claim 6. As indicated in the discussion above, the signal production circuit of claim 6 is not disclosed, described, taught or suggested in the combination of Suzuki, Lill and Yoshida. Applicant also submits that this combination of references also does not provide any teaching, suggestion nor offer any motivation for modifying the signal

production circuitry disclosed in Suzuki so as to yield the signal production circuitry of claim 6. As such, at least because of its dependency from an allowable claim, claim 6, claim 18 also is believed to be allowable.

Claim 19 depends from claim 9. As indicated in the discussion above, the signal production circuit of claim 9 is not disclosed, described, taught or suggested in the combination of Suzuki, Lill and Yoshida. Applicant also submits that this combination of references also does not provide any teaching, suggestion nor offer any motivation for modifying the signal production circuitry disclosed in Suzuki so as to yield the signal production circuitry of claim 9. As such, at least because of its dependency from a base claim that is believed allowable, claim 19 also is believed to be allowable.

As to the fourth reference of the cited combination, Farla, this reference is being cited for the limited purpose of allegedly teaching the additional limitations of each of claims 14-15, 18 and 19. It necessarily follows therefore that Farla cannot overcome the shortcomings pointed out above regarding the combination of Suzuki, Lill and Yoshida.

Applicant would note that the foregoing should not be interpreted as or be understood to be a waiver of any argument as to the appropriateness of the suggested combination of Suzuki and the teachings of Lill and Yoshida with Farla. Applicant believes that Examiner has not provide a sufficient basis as to why one skilled in the art of designing circuits for display apparatuses would have been motivated to use the various techniques disclosed in Suzuki, Lill,

Yoshida and Farla. In this regard, Applicant also refers to the more detailed remarks regarding this particular point as provided hereinabove.

It is respectfully submitted that claims 14-15, 18 and 19 are patentable over the cited reference(s) for the foregoing reasons.

The following additional remarks shall apply to each of the above.

The Federal Circuit has indicated in connection with 35 U.S.C. §102 that in deciding the issue of anticipation, the trier of fact must identify the elements of the claims, determine their meaning in light of the specification and prosecution history, and identify *corresponding elements* disclosed in the allegedly anticipating reference (emphasis added, citations in support omitted). *Lindemann Maschinenfabrik GMBM v. American Hoist and Derrick Company et al.*, 730 F. 2d 1452, 221 USPQ 481,485 (Fed. Cir. 1984). Notwithstanding that the instant rejection is under 35 U.S.C. §103, in the present case the Examiner has not shown that the shift register, the latch circuit and the arrangement of these elements in Suzuki, alone or in combination with the other cited art, corresponds, as that term is used above by the Federal Circuit, in any fashion to the storage means, the serial-to-parallel converter means and the arrangement of the storage means and the serial-to-parallel converter means in its entire claimed form as set forth in any of the independent claims of the present invention.

As provided by the Federal circuit, a 35 U.S.C. §103 rejection based upon a modification of a reference that destroys the intent, purpose or function of the invention disclosed in a

reference, is not proper and the prima facie case of obviousness cannot be properly made. In short there would be no technological motivation for engaging in the modification or change. To the contrary, there would be a disincentive. *In re Gordon*, 733 F. 2d 900, 221 USPQ 1125 (Fed. Cir. 1984). In the present case it is clear that if electron beam generating device/ apparatus disclosed in Suzuki was modified in the manner suggested by the Examiner, as well as that allegedly taught in either of Lill, Yoshida and/ or Farla, it would destroy the intent, purpose or function of the device as taught by Suzuki.

Although a prior art device "may be capable of being modified to run the way the apparatus is claimed, there must be a suggestion or motivation in the reference to do so." *In re Mills*, 916 F. 2d, 680, 682; 16 USPQ 2d 1430, 1432 (Fed. Cir. 1990). See also *In re Fritch*, 972 F. 2d 1260, 23 USPQ 2d 1780 (Fed. Cir. 1992).

As the USPTO Board of Patent Appeals and Interferences has held, "The mere fact that a worker in the art could rearrange the parts of the reference device to meet the terms of the claims on appeal is not by itself sufficient to support a finding of obviousness. The prior art must provide a motivation or reason for the worker in the art, without benefit of appellant 's specification, to make the necessary changes in the reference device." *Ex parte Chicago Rawhide Mfg. Co.*, 223 USPQ351, 353 (BD. Pat. App. & Inter. 1984). It is clear from the foregoing remarks that the suggested modification to the electron beam generating device disclosed in Suzuki would require a modification to the operation of the disclosed device and/or is more than an obvious matter of design choice.

It is respectfully submitted that for the foregoing reasons, claims 1-21 are patentable over the cited reference(s) and thus, satisfy the requirements of 35 U.S.C. §103. As such, these claims are allowable.

CLAIMS 22-26

As indicated above, claims 22-26 were added to more distinctly claim embodiments/ aspects of the present invention. These claims are clearly supported by the originally filed disclosure, including the originally filed claims. It also is respectfully submitted that these added claims are patentable over the cited prior art on which the above-described rejection(s) are based.

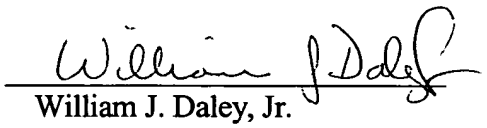
It is respectfully submitted that the subject application is in a condition for allowance. Early and favorable action is requested.

Applicant believes that additional fees are not required for consideration of the within Response. However, if for any reason a fee is required, a fee paid is inadequate or credit is owed

for any excess fee paid, the Commissioner is hereby authorized and requested to charge Deposit Account No. **04-1105**.

Respectfully submitted,
Edwards & Angell, LLP

Date: August 9, 2004

By: 

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